Master thesis

» Analysis and Design of Current-mode Sampler in 130nm BJT Technology «

The research group
Circuit and System Technology
offers a Master thesis

The push for higher data rates drives the need for cost-effective solutions, especially for ADCs in receiver paths. While CMOS ADCs can be parallelized for higher sampling rates, scaling them for higher analog bandwidths remains challenging. Hybrid integration of front-end circuits as bandwidth gearboxes in other semiconductor technologies offers a promising research direction.

Task Description:

- Literature review of various topologies for Current-mode samplers. Comparison of topologies analytically and by simulation. The circuits are to be designed in SG13G3_Cu technology from IHP
- A chip layout with DRC- and LVS-clean is expected along with post-layout analysis such as RC and EM simulation.
- Comparison of the results with best-in-class current-mode samplers.
- In conclusion, an assessment of the work and a forward-looking perspective should be provided. The anticipated outcomes of circuit enhancements should be examined.

Requirements:

- CV and Transcripts.
- Lectures: Circuit & System Design plus at least one subject with high-frequency engineering contents
- At least one project in our department with circuit emphasis.
- Experience in CADENCE Virtuoso or ADS is mandatory.

In case of interest, please send an e-mail containing your latest transcript of records, cv etc., to Harshan Gowda (harshan@hni.upb.de)

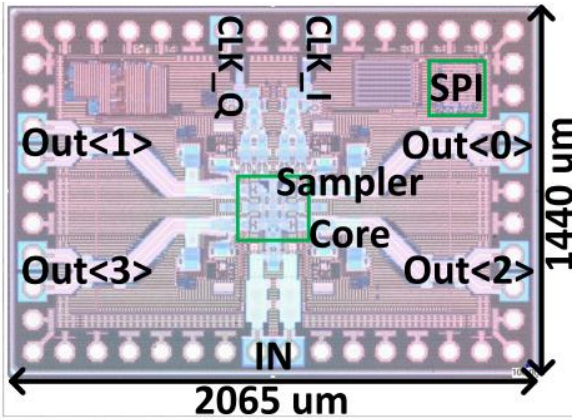

Figure 1: Current mode sampler IC [1].

[1S. Niu *et al.*, "A 200–256-GS/s Current-Mode 4-Way Interleaved Sampling Front-End With Over 67-GHz Bandwidth Using a Slew-Rate Insensitive Clocking Scheme," in *IEEE Journal of Solid-State Circuits*, doi: 10.1109/JSSC.2024.3416528.

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