Master thesis

» Design and Implementation of a Class-F CMOS Oscillator in 22nm FD-SOI Technology«

The research group Circuit and System Technology offers a Master thesis:

Task Description:

- The thesis begins with comprehensive study of fundamentals of oscillators, phase noise, LC characteristics, and transformers.
- In the second step, the phase noise analysis will be investigated in depth based on Impulse Sensitivity Function (ISF) model.
- The third part includes literature review of different types of LC oscillators with focus on class-F architecture.
- In the fourth part of this thesis different blocks of oscillator including: transformer, cross-coupled pair, and switch capacitor bank are designed and implemented using Cadence/ADS tools.
- Finally, the implemented circuit should be evaluated and compared to previous arts and propositions should be offered to further improve the design in future.

Requirements:

- Lectures: Circuit & System Design plus at least one subject with high-frequency engineering content.
- Participating in at least one project group in Circuit and System department.
- Experience in CADENCE Virtuoso is mandatory.

In case of interest, please send an e-mail containing your CV and latest transcript of records to Babak Sadiye (babaks@hni.uni-paderborn.de).

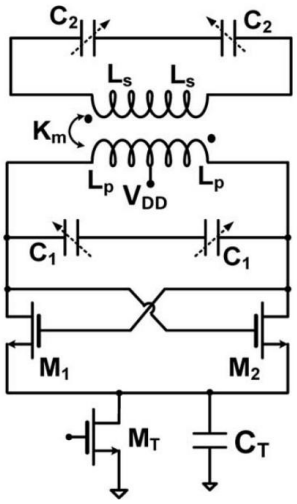

Figure 1: Schematic of a class-F oscillator [1].

[1] M. Babaie and R. B. Staszewski, "A Class-F CMOS Oscillator," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3120-3133, Dec. 2013.

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