Master thesis

» Investigation and design of a transimpedance amplifier for coherent receivers in 22nm CMOS technology «

The research group Circuit and System Technology offers a Master thesis

Task Description:

- A comprehensive literature review and investigation on the Coherent detection, different topologies of transimpedance amplifier, variable gain amplifier and buffer.
- Design and simulation of the blocks in 22nm CMOS technology containing schematic design, Layout and post layout simulations and EM simulation.
- Finally, an evaluation of the work as well as an outlook should be given. Circuit improvements should be analyzed in regards to their expected results.
- Regular Reports are expected.

Requirements:

- CV and Transcripts.
- Lectures: Circuit & System Design.
- Familiarity with optical circuits design or lecture “Fast integrated circuits for wireline communication”.
- At least one project in our department with circuit emphasis.
- Experience in CADENCE Virtuoso or ADS is mandatory.

In case of interest, please send an e-mail containing your latest transcript of records to Armin Amirkhani (arminam@hni.uni-paderborn.de)

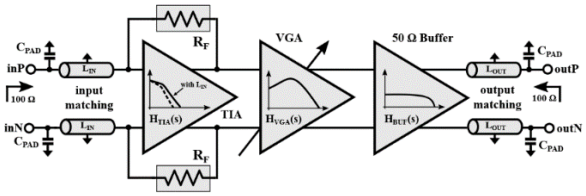

Figure 1: example on block diagram of the main chain [1].

[1] I. García López, A. Awny, P. Rito, M. Ko, A. C. Ulusoy and D. Kissinger, "100 Gb/s Differential Linear TIAs With Less Than 10 pA/$\sqrt{Hz}$ in 130-nm SiGe:C BiCMOS," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 458-469, Feb. 2018

Circuit and System Technology
Prof. Dr.-Ing. C. Scheytt

Contact: Armin Amirkhani
Mail: arminam@hni.uni-paderborn.de